# Data Device Corporation



## Multi-Protocol PCI Card

## NHi-15504
## Instructions

### Version 3.0
### September 2004



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## 1.0 Package Contents

One PCI card
Instructions
Software Disks: WindowsNT/XP/98/2000/ME Flight Deck Software
PCI504.exe GUI Application
PCIhlp.txt Help file for GUI application
Man156XX.pdf NHI-15625ET manual
15504man.pdf card instructions

Flight Deck is menu driven GUI software which controls the PCI card and all the functions of the multi-protocol terminal on the card.

NHi-156XXMan.pdf is the manual for the NHi-15625ET terminal which is on the PCI card.

## 1.1.0 GENERAL TERMINAL FEATURES

- Multi-Protocol Interface
- Operates from 20 Mhz clock.
- Appears to host as a Dual Port Double Buffered 64K x 16 SRAM
- Footprint less than 1 square inch
- Ensures integrity of all shared data and control structures
- Built- in interrupt controller
- Internal FIFO is configurable to retain header information for queuing up to 6 pending interrupt requests plus an overflow interrupt, or as a 7 interrupt revolving FIFO
- 32 bit RTC (Real- Time- Clock) for time taging with 1, 2, 4, 8,1 6, 32 and 64 uS selectable tick rate, for data and event time tagging.
- Selectable 768/ 672 us Failsafe Timer with complete Testability.
- Double buffering of messages and data tables.
- Low power CMOS technology

### 1.1.1 BUS CONTROLLER FEATURES

- Implements all Message Formats and Error Checking
- Major and minor frame message structure.
- Simple setup and operation. Multiple minor frames, message tables and data tables. Only one Major Frame Pointer Register is required to control unlimited number of messages
- BC initialized by writing to three Configuration Registers and the Interrupt Mask Register
- Executes lists of messages via Minor Frame Pointers
- Configurable Global Retry and Message Specific Local Retry
- Programmable retries per message:
  - None
  - Retry Current Bus
  - Retry Alternate Bus
  - Retry Alternate Bus then Current Bus.
- Programmable response timeout of 14, 18, 26, or 42 microseconds.
- Programmable Intermessage Gap Time up to 4 mS with 2uS resolution.
- Programmable Synchronous Message Time up to 4mS with 2uS resolution.
- Extended Gap Time and Synchronous Message Time using NO- OP Feature.
- Programmable Minor Frame Gap with 64 us resolution.
- Programmable Interrupts for:
  - End of Message
  - End of Frame
  - Response Time Out, Message
  - Error
  - Message Retry
  - RT Status Bit Set
  - FIFO Overflow.
- Host controlled commands:
  - Start BC
  - Continuous Mode
  - Stop at End of Message
  - Stop at End of Frame
  - Abort,
  - GOTO Alternate Frame.
- Dynamic Message Bus Switch Upon Successful Retry.
- Synchronous or Asynchronous Messages.
- Synchronous or Asynchronous Minor Frames.
- Up to 63 autonomous data tables per message.

### 1.1.2 REMOTE TERMINAL FEATURES

- Up to 63 autonomous data tables per message.
- Multiple and individual message logs provide expedited message analysis.
- Asynchronous Message Handling.
- Dynamic Bus Control Acceptance
- Message Illegality is internally programmable.
- Employs data tables with individual tag words which indicate data validity, data latency, table status and broadcast
- Optionally sets the subsystem flag bit whenever stale data is transmitted or received data is overwritten.
- Issues interrupts on any subset of T/ R bit, subaddresses, mode commands, broadcast messages and errors.
- Optionally resets the real- time clock in response to a "Synchronize" mode command.
- Optionally updates the lower 16 bits of the real- time clock in response to a "Synchronize With Data" command.
- Internally loops- back messages under host control for test purposes.
- Employs a decoder algorithm which ensures high noise immunity and a low error rate.
- Software RT Address Lockout.
- MDC3818 Status Response, Error Handling, Status Bit Definition, Mode Code Operation.
- Separate Broadcast Tables and Interrupts.

### 1.1.3 BUS MONITOR FEATURES

- Simple setup and operation
- Preset multiple data blocks.
- Only one MT Data Start Address Register is required to control unlimited number of message blocks. The data block sizes and locations are totally programmable.
- MT initialized by writing to three MT Configuration Registers and the MT Interrupt Mask Register.
- Error detection and reporting
- All encoding, timing and protocol errors defined by the Protocols are detected.

- Programmable Monitor Modes:
  - Word Monitor, transfers all data with/ without ID and Time Tag words.
  - Message Monitor, transfers all Command and Status words with/ without ID and Time Tag，while data words are transferred directly to conserve memory space.
- Concurrent Bus Monitor and Remote Terminal operation.
- Selective Message Monitor, based on RT Address.
- Programmable Interrupt for End of Block.

## 1.2 Description

The NHi-15504 is a PCI card which contains a completely independent 1553 interface. The interface uses a NHi-15625ET multi-protocol MCM . which can operate as an RT, BC, or MT.
The ET includes two monolithic transceivers, a protocol asic and 64K words of shared RAM. Double buffering of the shared RAM enables simultaneous message preparation
and 1553 bus transfers.

All modes of operation access data tables via pointers residing in RAM which
facilitates multiple buffering. This allows buffers to change without moving data and promotes efficient use of RAM space. The data tables have programmable
sizes and locations.

The invisibility of memory when the card is not active prevents inadvertent access
during power-on-self test of the PC or by any other process.

## 2.0 Inspection

The card has been thoroughly tested and inspected before shipment. After removing the
card from the packing container, please retain the container as it may be used to store the
card when not installed in the computer. The packing container may be utilized in the event that the card has to be returned due to failure or damage.

## 2.1 System Requirements

PC with PCI Bus
Windows2000/ME/XP/98/NT
Hard disk
Color Monitor

Follow these precautions before installing the card inside your PC. Remove power to the
PC before opening the top cover. Make the necessary switch and jumper selections for your application as detailed in this manual and then plug the card into an available slot on the motherboard.
The card has been delivered from the factory with the following default settings:

IRQ from the terminals are software disabled.
Hardwire RT address 01 (via jumper blocks).

## 2.2 Installation

**REMOVE POWER TO THE PC WHEN REMOVING OR INSERTING THE CARD INTO THE PC.**

From a subdirectory on the floppy disk, copy all the files for the Windows operating system on the PC into a convenient subdirectory on the hard disk, such as:

C:\NHi15504pci

Also copy the files PCI504.exe, PCIhlp.txt, 15504man.pdf and Man156XX.pdf into this directory.
Turn off PC and install the NHi-15504PCI card.

Turn on PC.

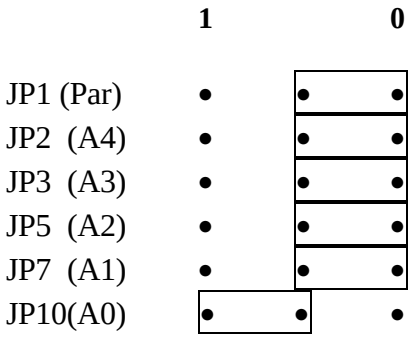
Windows Plug'n'Play should detect the new hardware. Do NOT let Windows look for a driver. Direct Windows to the subdirectory where the driver resides, C\NHi15504pci in this example.

NOTE:
For windows NT which is not Plug'n'Play, follow the installation instructions in the .txt file which came with the NT driver files.

## 2.3 Hardwired RT Address Jumpers

The Terminal can be given a unique Remote Terminal(RT) hardwire address via jumper selection.

The Factory default configuration for a terminal with an RT address of 1 and odd parity is shown below:

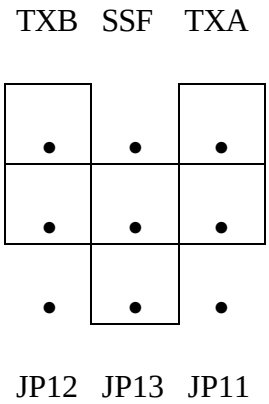



**Note**:
In the above illustration, position the PCI card with the component side up and the Bus connectors on your left.

## 2.4 TRANSMITTER ENABLE AND SUB-SYS FLAG INPUTS

Defintions
JP11-Enables/disables Transmitter "A
JP12-Enables/disables Transmitter "B
JP13-Enables/disables Sub-sys Flag Input

The Factory default configuration for having both transmitters enabled and the SSF disabled is shown below:



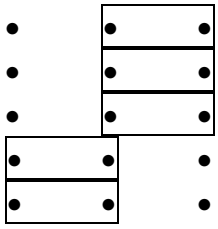

## 2.5 **MASTER RESET AND IRQ JUMPERS**

**Definitions** (Ref:Reset/IRQ circuit below)
JP4---This jumper determines whether or not an External INTA is allowed from the PCI bus.
JP14--This jumper determines whether or not a resistor (300 ohms) is allowed in series with the Master Reset line.
JP6---This jumper determines whether or not an External Reset is allowed from the PCI bus.
JP8---This jumper determines whether 3.3v or 5.0v is used to pull up the reset line if desired.
JP8---This jumper determines whether or not C3 (.01uf) is needed for filtering on the reset line.

Default

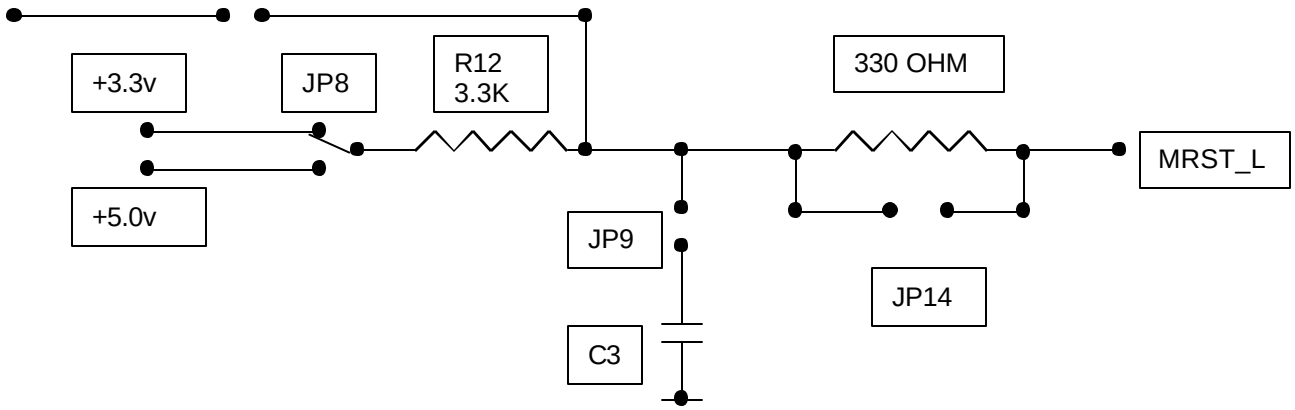
The factory default configuration fot the IRQ line and RESET line is as follows:

JP4 (Open)
JP14 (Open)
JP6 (Open)
JP8 (3.3V)
JP9 (C3 Open)



RESET/IRQ Reference Circuit:

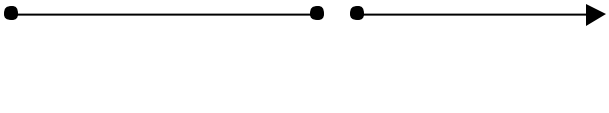
**PCI-A15**




**RST_L** JP6

Ground

**PCI-A6**
**INTA_L** JP4



IRQ

## 3.0 ADDRESS MAP

The following memory map information is not generally required by a user unless custom software is being developed for the NHi PCI card.. The NHi Flight Deck Windows software handles all memory allocation and accesses.

The terminal on the 15504 card appears to the host as 64K words of contiguous memory. The address map for the terminal is shown below.

ADDRESS (in blocks)

| | |
|---|---|
| 0-31 | Internal Control and Status registers |
| 32-63 | Reserved |
| 64- 65535 | Shared RAM |

The following address map table defines all addresses relevant to the user. The addresses are offsets from the base address as selected by the user.

| ADDRESS | CONTENTS/OPERATION | R/W |
|---|---|---|
| Base + 0 | Control Register | R/W |
| Base + 1 | RT Message Pointer Table Address Register | R/W |
| Base + 2 | Basic Status Register | R/W |
| Base + 3 | INTERRUPT MASK (lower byte) | R/W |
| Base + 3 | INTERRUPT VECTOR REQUEST (upper byte) | R |
| Base + 3 | INTERRUPT REQUEST (upper byte) | W |
| Base + 4 | INTERRUPT VECTOR (lower byte) | R/W |
| Base + 4 | AUXILLARY VECTOR (upper byte) | R |
| Base + 4 | Configuration Register 2 (upper byte, BC/MT only) | W |
| Base + 5 | REAL TIME CLOCK_ High Word | R |
| Base + 6 | REAL TIME CLOCK _ Low Word | R |
| Base + 7 | REAL TIME CLOCK Control | R/W |
| Base + 8 | Read FIFO | R |
| Base + 8 | Reset FIFO | W |
| Base + 9 | Configuration 1 | R/W |
| Base + 10 | BC Current Major & Minor Frame Index | R |
| Base + 11 | Last Command | R |
| Base + 12 | Last Status | R |
| Base + 13 | Major Frame “A” Address | R/W |
| Base + 14 | Asynchronous Frame Address | R/W |
| Base + 15 | Reset Terminal (both bytes) | W |
| Base + 16 | Major Frame “B” Address | R/W |
| Base + 17 | Reserved | |

| ADDRESS | CONTENTS/OPERATION | R/W |
|---|---|---|
| Base + 18 | Encoder Status | R |
| Base + 19 | Condition | R |
| Base + 20 | BC Frame Gap/ Word Mtu End of Frame Options | R/W |
| Base + 21 | Configuration 3 | R/W |
| Base + 22 | Message Monitor Address Filter (0-15) | R/W |
| Base + 23 | Encoder Data * | R/W |
| Base + 24 | Encoder Data TX Request * | W |
| Base + 25 | Encoder CMD TX Request * | W |
| Base + 26 | Message Monitor Address Filter (16-31) | R/W |
| Base + 27 | Monitor Block "A" Last address | R |
| Base + 27 | Clear register 27 | W |
| Base + 28 | Monitor Block "B" Last Address | R |
| Base + 28 | BC current message Address | R |
| Base + 28 | Clear register 28 | W |
| Base + 29 | RT Log Pointer Table Address | |
| Base + 30 | External RT Address Buffer (lower byte) | R |
| Base + 30 | Reserved | |
| Base + 31 | BC & MT Interrupt Vector | R/W |

* In order to write to addresses 23, 24, and 25, the Terminal must be in loopback in the RT mode (see Control Register for details.

# 4.0 HARDWARE DESCRIPTION

## 4.1 Clock

A 20 Mhz oscillator (U3) is used to provide the required clocks for the NHi-15504 PCI Card.

## 4.2 NHi-15625ET Terminal

The PCI card contains one NHi-15625ET terminal, which functions as a BC, MT, RT or an MT/RT. See the NHi Enhanced Terminals Manual for a full description.

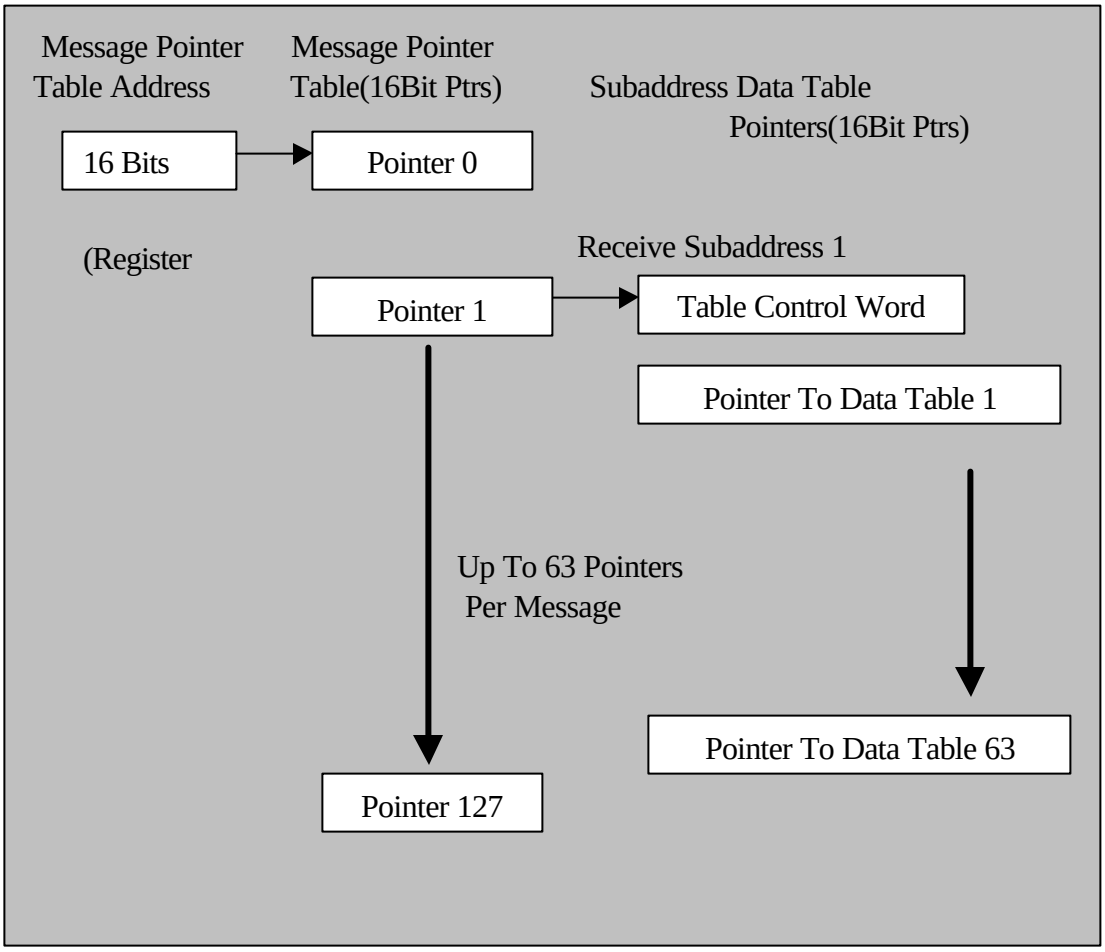
# 5.0 On-Line Help

On-Line help is available for all menu items and dialog boxes. Use the left mouse button to drag the Question Mark(?) to the item requiring help; then release the button over that item. The help dialog will appear in the upper left screen area.

## 6.0 NHi-15504PCI MEMORY STRUCTURE

REMOTE TERMINAL MEMORY ORGANIZATION

The T/R bit subaddress and word count fields in the Command word are used to index into a message Pointer table as defined below:

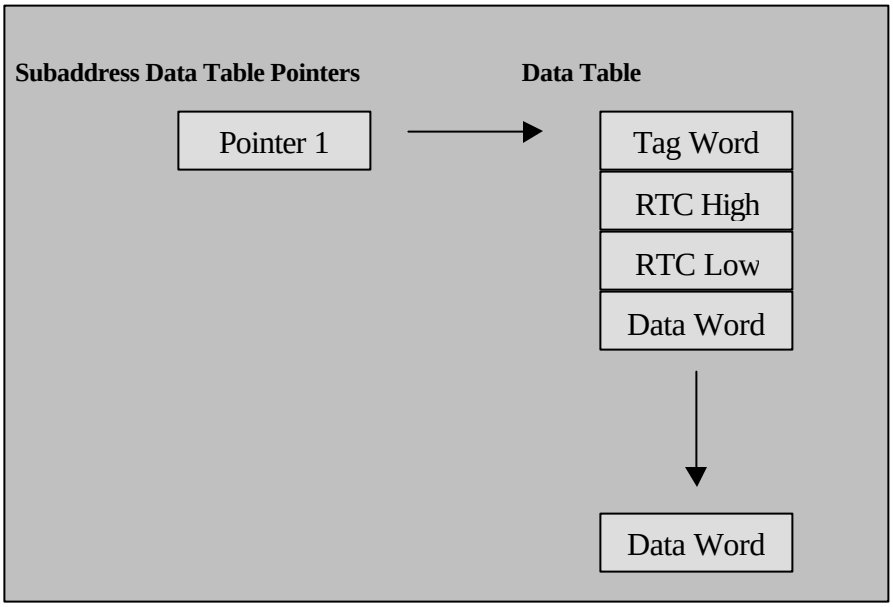



**MESSAGE POINTER TABLE INDEX**

| Index | T/R | Subaddress | Mode Code | Command |
|---|---|---|---|---|
| 0 | | Not Used | | |
| 1 - 30 | 0 | 1 - 30 | | Receive/Bcst |
| 31 | 0 | 31 (Note 2) | | Receive/Bcst |
| 32 | | Not Used | | |
| 33 - 62 | 1 | 1 - 30 | | Transmit |
| 63 | 1 | 31 (Note 2) | | Transmit |
| 64 - 95 | X | 0,31 (Note 2) | 0 - 31 | Mode Code |
| 96 | | Not Used | | |
| 97 - 126 | 0 | 1 - 30 | | Broadcast |
| 127 | 0 | 31 (Note 2) | | Broadcast |

Note : Broadcast messages may be separate or combined with Receive.

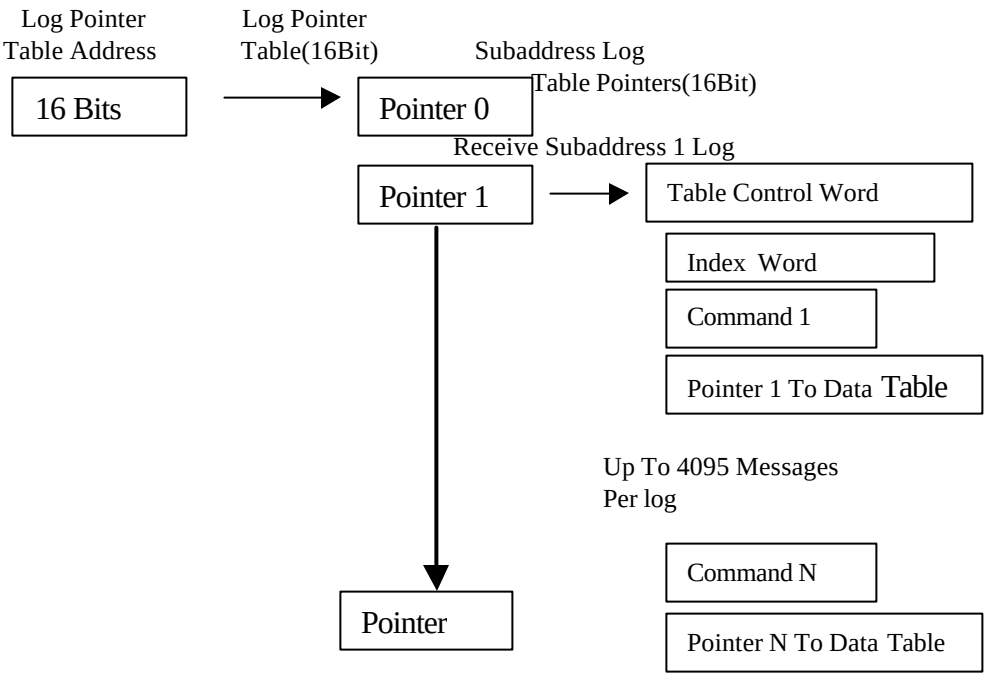
REMOTE TERMINAL DATA TABLE ORGANIZATION




**REMOTE TERMINAL DATA TABLE TAG WORD**

| **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** |
|---|---|---|---|---|---|---|---|
| UPDATE | SSFENA | BCST | INTREQ | LOCATION | PULSE2 | PULSE1 | PULSE0 |
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| LOCK | INVALID | OVRWRT | WCNT4 | WCNT3 | WCNT2 | WCNT1 | WCNT0 |

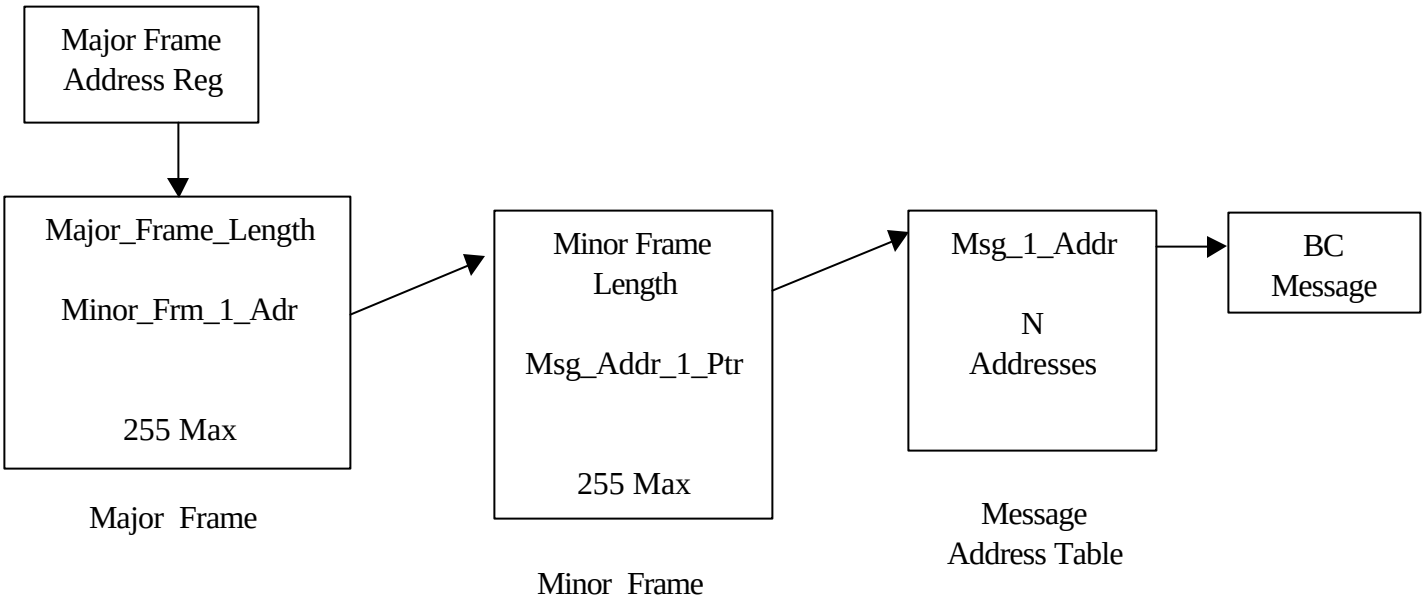
### 6.2.0 REMOTE TERMINAL MESSAGE LOG FORMAT



**BUS CONTROLLER MEMORY ORGANIZATION**

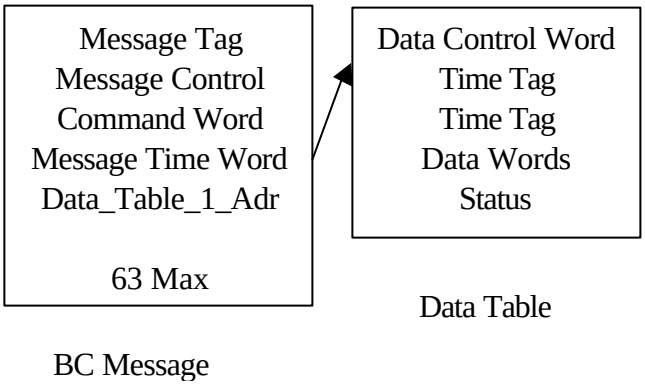
The message concept employs major and minor frames, message address tables, BC messages and data tables. This approach provides the BC with flexibility, autonomy and data buffering.

**BCU FRAME STRUCTURE**

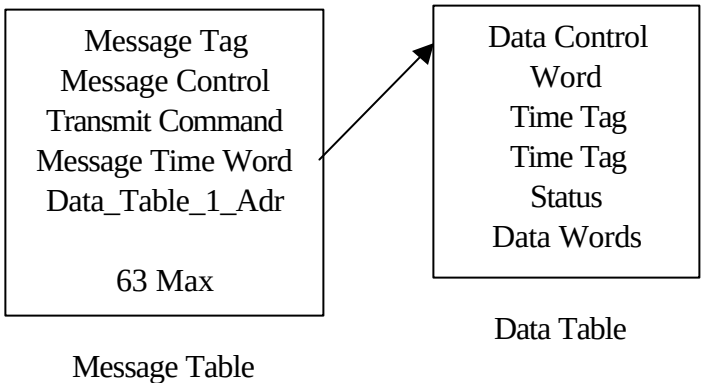



**Message Structures**

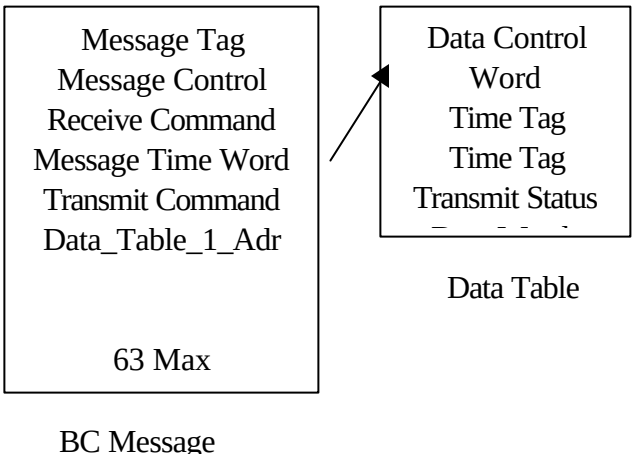
**Receive Command**



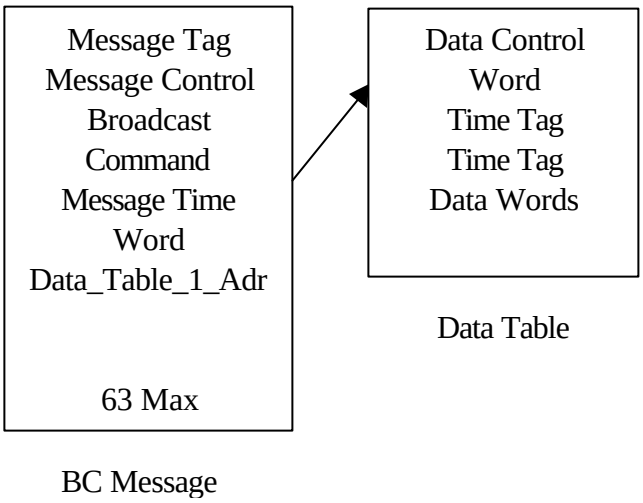

**Transmit Command**



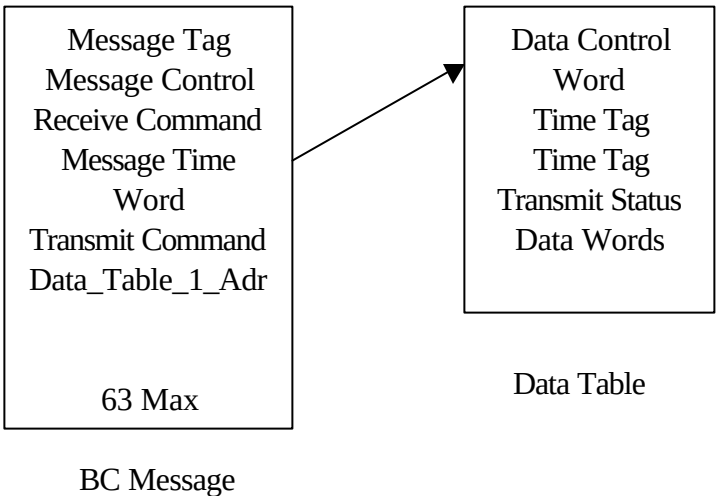
**RT-RT Command**



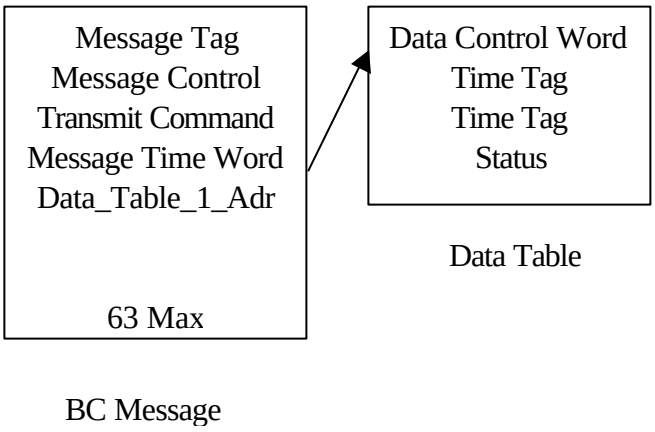

**Broadcast Receive C**ommand



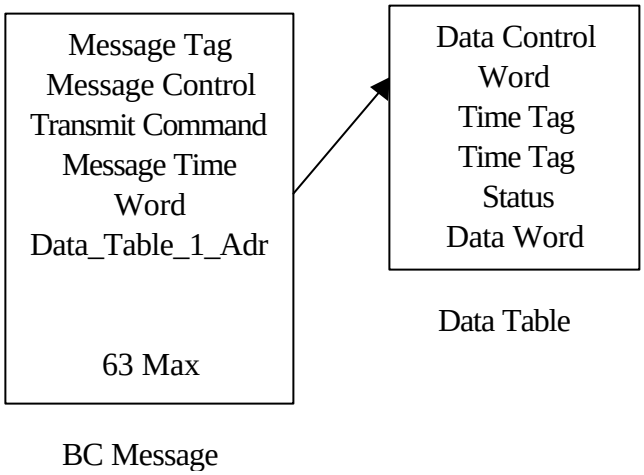

**Broadcast RT-RT Command**



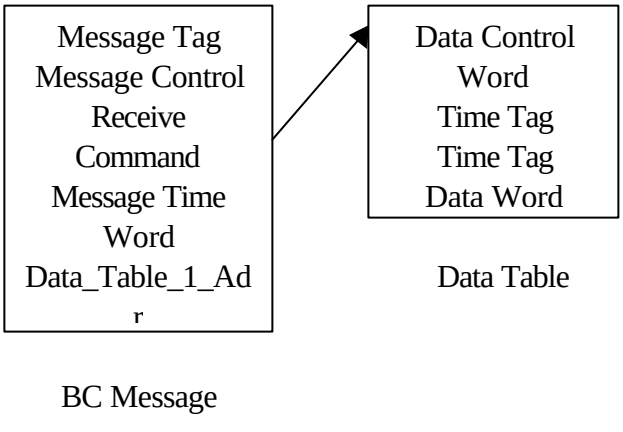
**Transmit Mode Code - No Data**



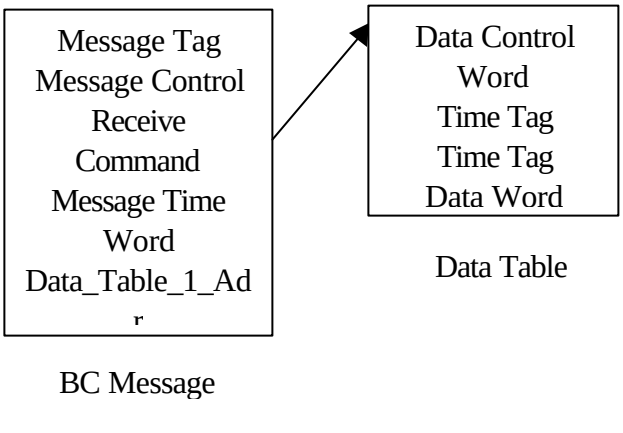

**Transmit Mode Code + Data**



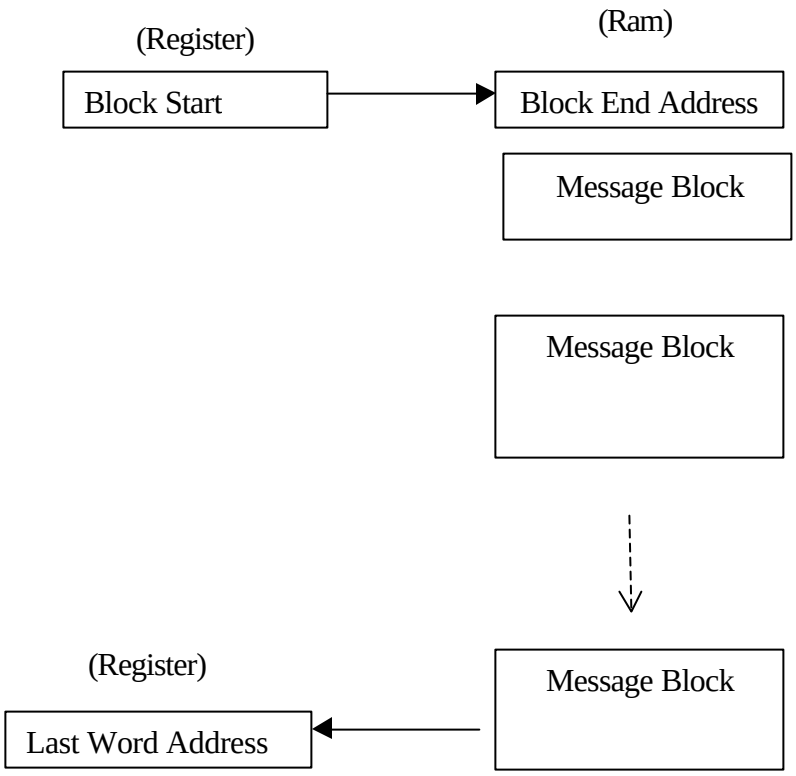

**Receive Mode Code**



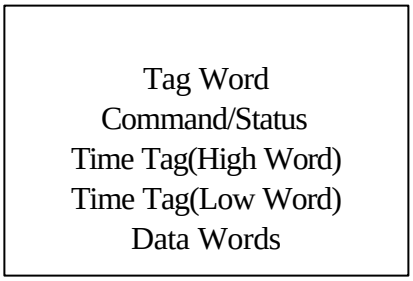

**Broadcast Mode Code**



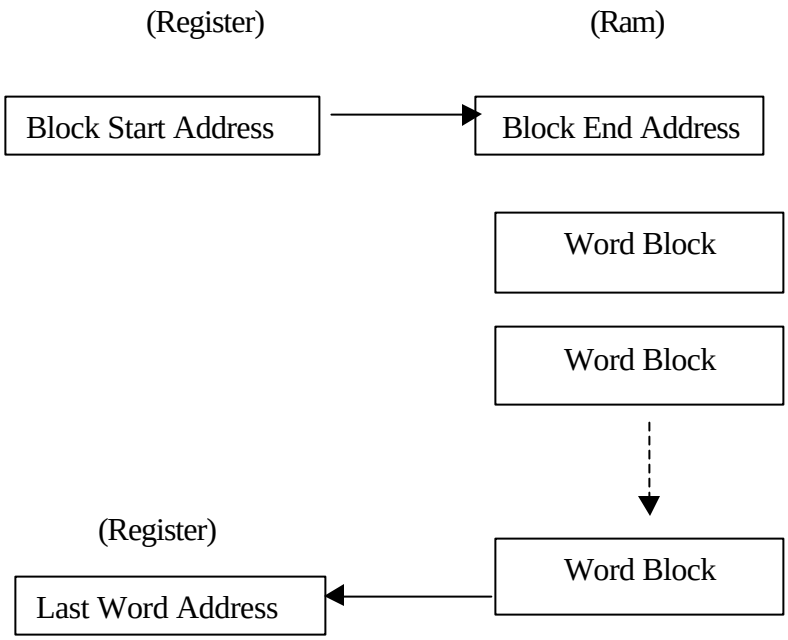
**MESSAGE MONITOR STRUCTURE**



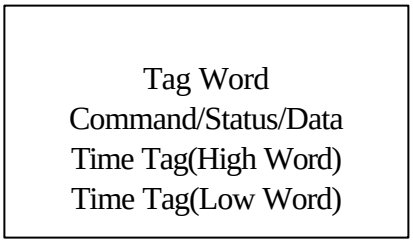

**MESSAGE MONITOR MESSAGE BLOCK STRUCTURE**



**Word Monitor Structure**




**WORD MONITOR WORD BLOCK ORGANIZATION**



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